Subclass	ISSUE CLASSIFICATION
Class	

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED 1084 Q.A.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/940472	F	327	36	2816	MINH NGUYEN

APPLICANTS: Katsuji Kimura

TITLE: Linear voltage subtractor/adder circuit and MOS differential amplifier circuit therefor

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	_____ (Primary Examiner) _____ (Date)			ISSUE FEE	
				Amount Due	Date Paid
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